Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-25 (Cancelled)

26. (Previously presented) A computer system comprising:

internal memory; and

an input/output section;

wherein the rate of input/output transactions in said input/output section is exponentially related to the amount of internal memory.

27. (Previously presented) The computer system of claim 26, wherein the relation between the rate of input/output transactions and the amount of memory includes an asymptotic limit for said rate of input/output transactions.

28. (Previously presented) The computer system of claim 26, wherein the relation between the rate of input/output transactions and the amount of memory includes a maximum rate of said input/output transactions.

29. (Currently amended) The computer system of claim 26 ~~3~~, wherein the relation between the rate of input/output transactions and the amount of memory includes:

a maximum rate of input/output transactions;

an asymptotic limit for said rate of input/output transactions; and

an exponential decay from said maximum transaction rate to said asymptotic limit as a function of an amount of said internal memory.

30. (Currently amended) The computer system of claim 29 [[27]], where said relation is in the form of $a+e^{(c+bx)}$, wherein a is said asymptotic limit, b represents said exponential decay, c represents a maximum rate of input/output transactions, and x represents the amount of memory.

31. (Previously presented) The computer system of claim 26 and further comprising at least one storage device to support said input/output transaction rate.

32. (Currently amended) The computer system of claim 31 [[29]] and further comprising at least one bus for communication between said storage device and said computer system to support said input/output transaction rate.

33. (Previously presented) The computer system of claim 31 [[29]] and further comprising at least one interface card to communicate with said storage device to support said input/output transaction rate.

34. (Previously presented) A method for manufacturing a computer system, said method comprising:

proving internal memory for said computer system; and

providing an input/output section for said computer system, wherein said input/output section has an input/output transaction rate associated therewith;

wherein said input/output transaction rate is exponentially related to the amount of said internal memory.

35. (Currently amended) The method of claim 34 [[32]], wherein the relation between said input/output transaction rate and the amount of said internal memory includes a parameter that defines an asymptotic limit for said input/output transaction rate.

36. (Currently amended) The method of claim 34 [[32]], wherein the relation between said input/output transaction rate and the amount of said internal memory defines a maximum input/output transaction rate.

37. (Currently amended) The method of claim 34 [[32]] wherein the relation between said input/output transaction rate and the amount of said internal memory includes a parameter that defines an exponential decay from a maximum transaction rate to an asymptotic limit as a function of the amount of memory.

38. (Currently amended) The method of claim 34 [[32]] wherein the relation between said input/output transaction rate and the amount of said internal memory includes is of the form: $a+e^{(c+bx)}$, wherein a is said asymptotic limit, b represents said exponential decay, c represents a maximum rate of input/output transactions, and x represents the amount of memory.

39. (Currently amended) The method of claim 34 [[32]] and further comprising providing at least one storage peripheral to support said input/output transaction rate.

40. (Currently amended) The method of claim 39 [[37]] further comprising providing at least one bus for communication between said storage peripherals and said computer system to support said input/output transaction rate.

41. (Currently amended) The method of claim 39 [[37]] further comprising providing at least one interface card to communicate with said storage peripherals to support said input/output transaction rate.